

FIG. 1

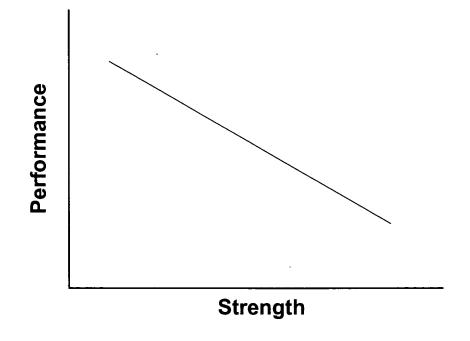


FIG. 2



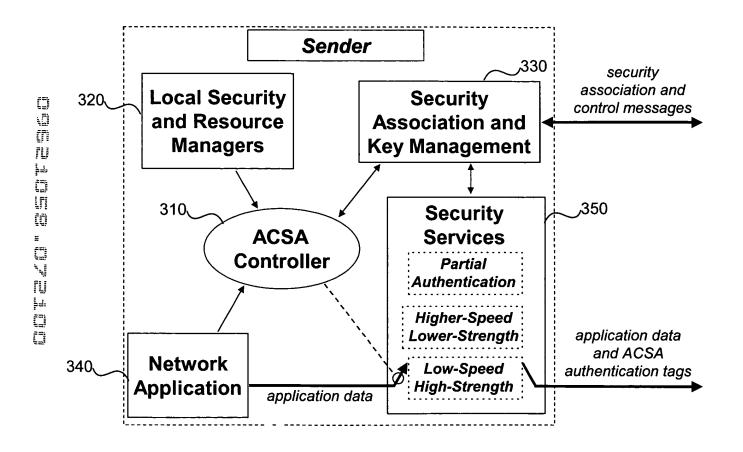


FIG. 3

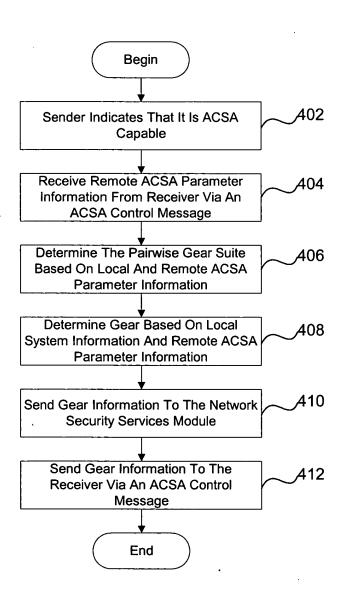


FIG. 4

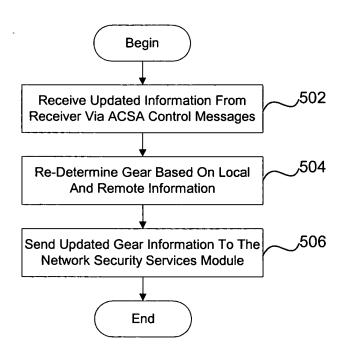


FIG. 5

Receiver Processor Utilization

		Too Heavily Loaded	Near Desired CPU Load	Lightly Loaded
Sender Processor Utilization	Too Heavily Loaded	switch to less computationally intensive gear	switch to less computationally intensive gear	switch to less computationally intensive gear
	Near Desired CPU Load	switch to less computationally intensive gear	maintain current gear	maintain current gear
	Lightly Loaded	switch to less computationally intensive gear	maintain current gear	switch to more secure (more computationally intensive) gear

FIG. 6

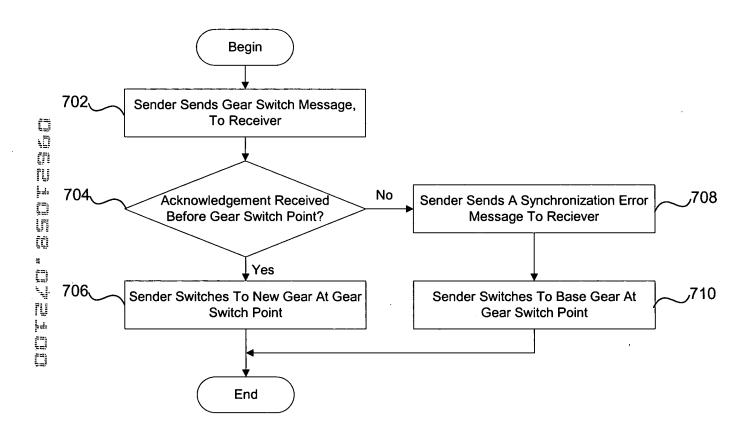


FIG. 7A

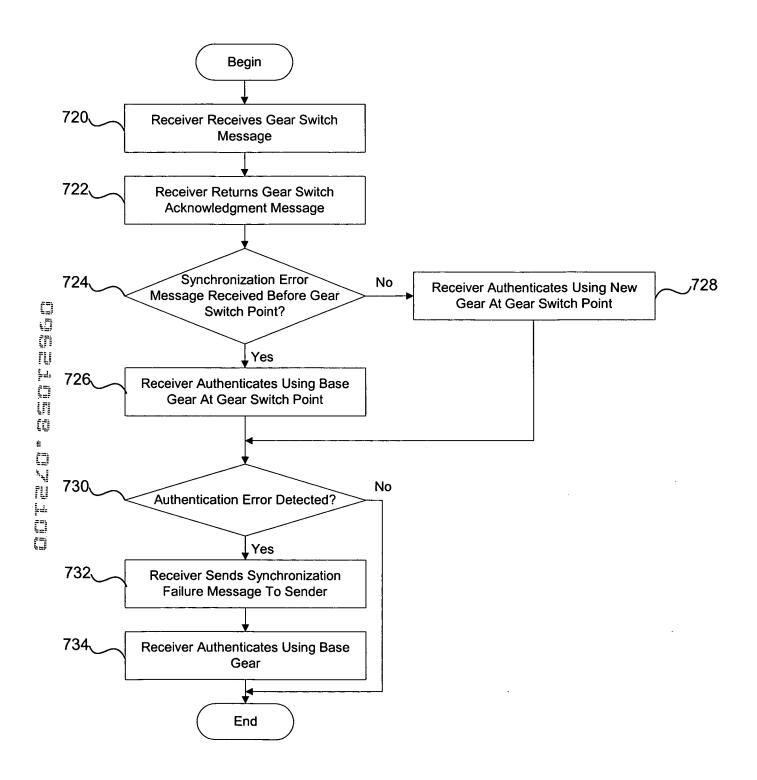


FIG. 7B

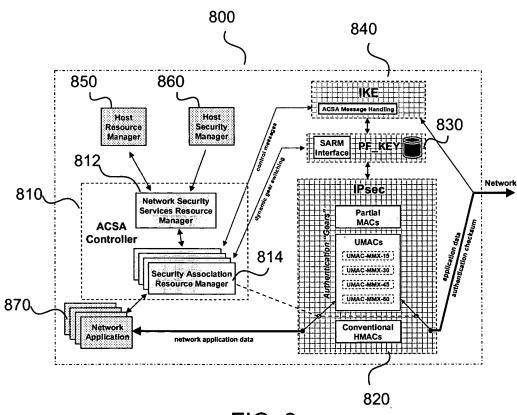
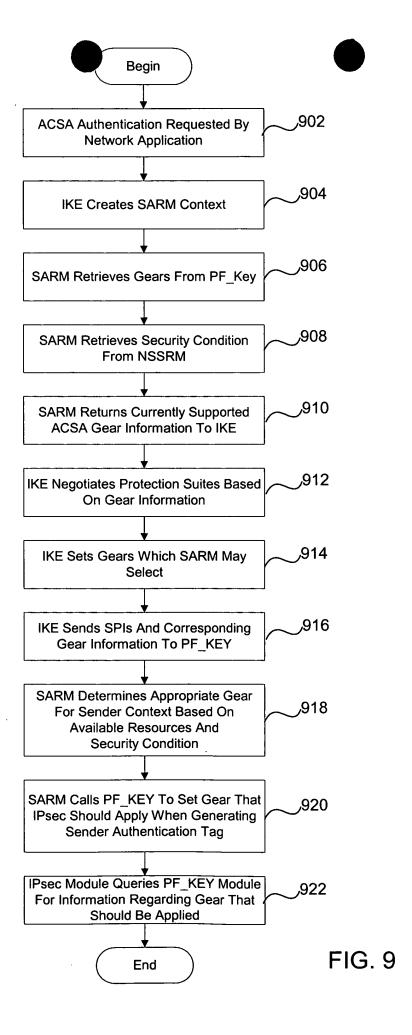


FIG. 8



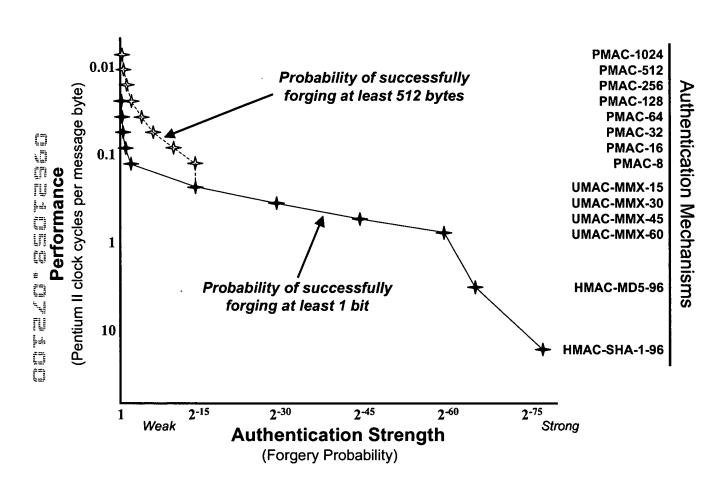


FIG. 10

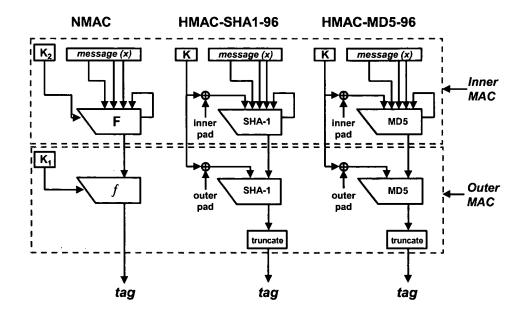


FIG. 11

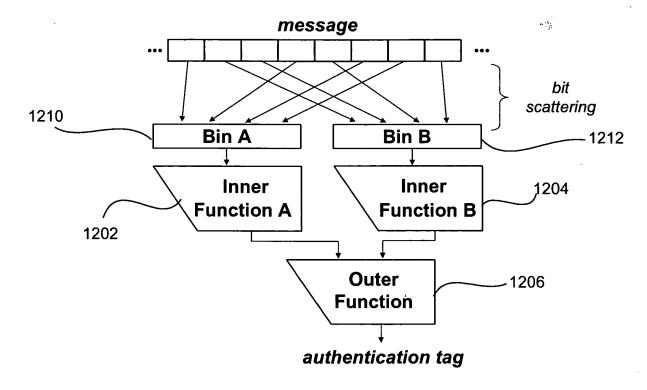


FIG. 12

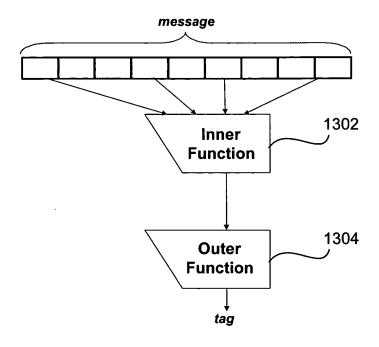


FIG. 13

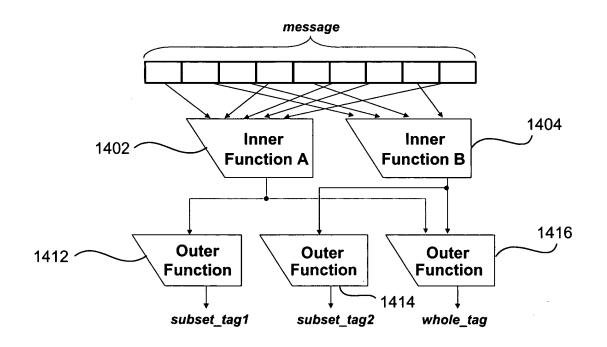
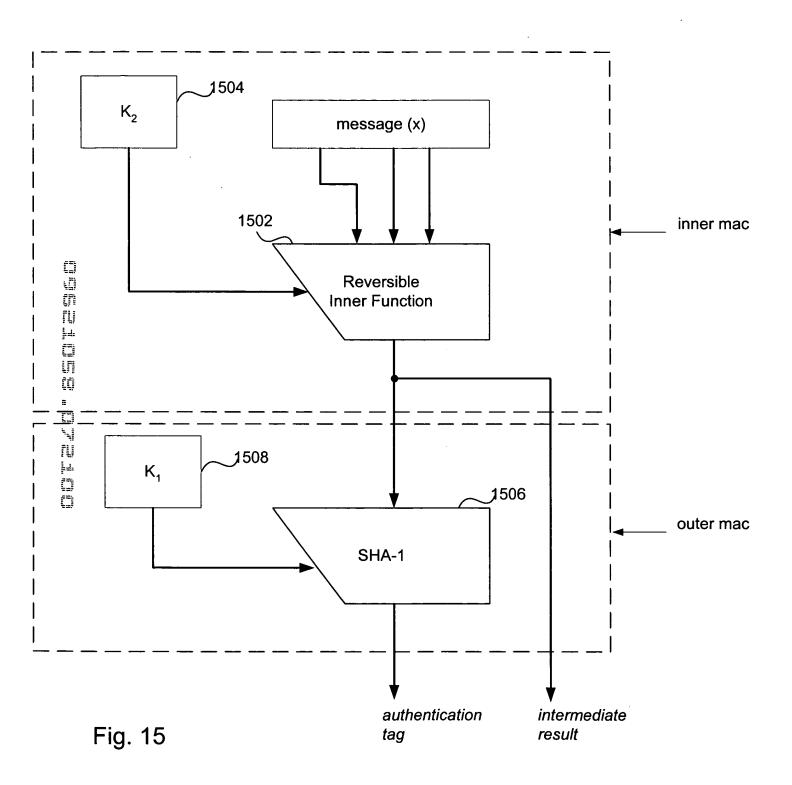
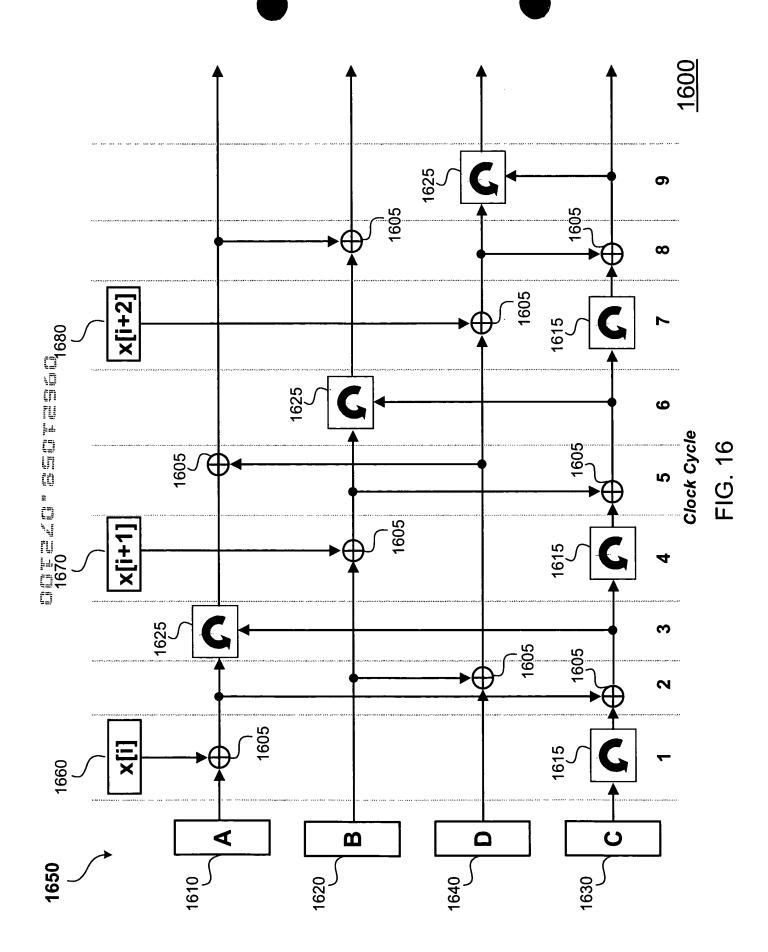


FIG. 14





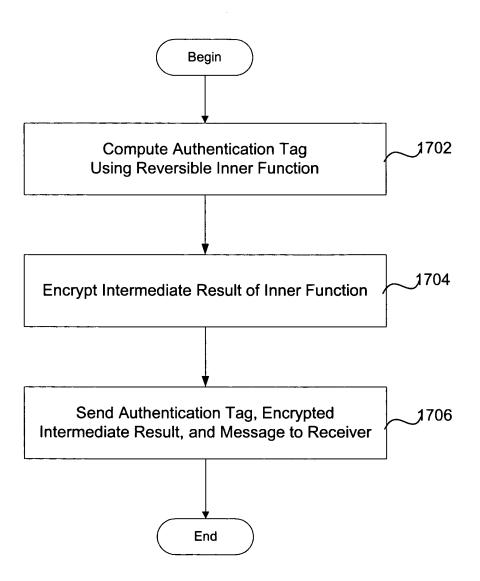


FIG. 17A

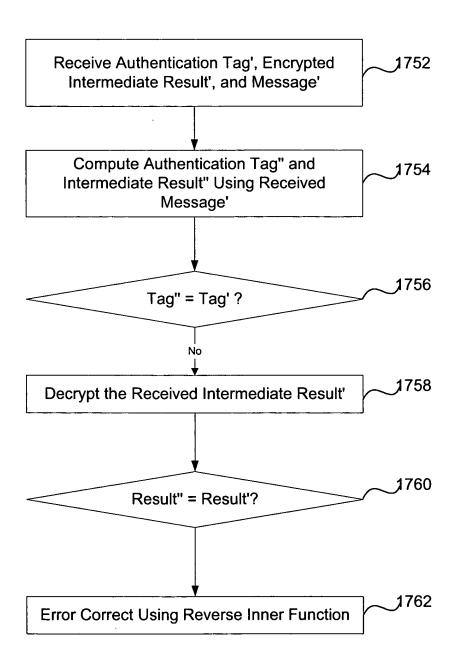


FIG. 17B